

**CLEAN SET OF CLAIMS**

What is claimed is:

- 1    25. A system, comprising:
  - 2       a memory array; and
  - 3       a memory array controller comprising:
    - 4           a negative charge pump; and
    - 5           a block controller coupled to the negative charge pump, comprising:
      - 6               a negative level shifter to switch an output between a read-mode voltage and
      - 7                 an erase-mode voltage dependent upon a selection signal input;
      - 8               a positive voltage switch coupled to the negative level shifter;
      - 9               a bit line driver coupled to the positive voltage switch and coupled to said
      - 10                 memory array; and
      - 11               a word line driver coupled to said positive voltage switch, coupled to the
      - 12                 negative level shifter, and coupled to said memory array.

1    26. The system of claim 25, wherein the negative level shifter comprises an output stage  
2       comprising an n-channel transistor.

1    27. The system of claim 25, wherein the negative level shifter comprises an active pull-up  
2       circuit coupled to a current source pull-down circuit.

1    28. The system of claim 25, wherein the erase-mode voltage comprises a high magnitude  
2       negative voltage.

1    29. The system of claim 25, wherein the read-mode voltage comprises a low voltage  
2       current from the negative charge pump via a low resistance n-channel transistor.

1    30. The system of claim 25, wherein said memory array comprises a block coupled to the  
2       block controller and having a bit line, a word line, and a source line.

1    31. The system of claim 25, wherein said memory array controller comprises the block  
2                          controller to apply a signal to a first block within said memory array to erase the first  
3                          block.

1    32. The system of claim 25, wherein said memory array controller comprises a second  
2                          block controller to apply a signal to a second block within said memory array to read a  
3                          memory cell of the second block substantially simultaneously with erasure of a first  
4                          block within said memory array.

1    33. The system of claim 25, wherein the negative charge pump comprises an output circuit  
2                          to output the erase-mode voltage.

1    34. The system of claim 25, wherein the negative level shifter comprises an output stage  
2                          circuit coupled to said memory array to apply the erase-mode voltage to a source line  
3                          of said memory array.

1    35. The system of claim 34, wherein the output stage circuit comprises a transistor to  
2                          couple the output of the negative charge pump to the source line.

1    36. The system of claim 25, wherein the negative level shifter comprises a first circuit to  
2                          pull up an output of the negative charge pump to apply a read-mode voltage to a first  
3                          memory cell of said memory array.

1    37. The system of claim 36, further comprising a second negative level shifter coupled to  
2                          the negative charge pump to couple the output of the negative charge pump to a second  
3                          memory cell of said memory array substantially simultaneously with the application of  
4                          the read-mode voltage to the first memory cell of said memory array.

1    38. The system of claim 36, wherein the first circuit comprises circuitry to substantially  
2                          prevent current burn within the negative level shifter.

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1      39. The system of claim 36, wherein the first circuit comprises an output stage circuit to  
2      apply a low resistance current to the first memory cell.

1    40. A method, comprising:

2                 receiving a signal to erase a first block within a memory array;

3                 lowering an output of a negative charge pump to a negative voltage;

4                 applying the output of the negative charge pump to a source line of the first

5                 block; and

6                 pulling up the output of the negative charge pump to apply a read-mode voltage

7                 to a memory cell of a second block within the memory array

8                 substantially simultaneously with said applying the output.

1    41. The method of claim 40, further comprising applying a signal to a word line and a bit

2         line to erase the first block.

1    42. The method of claim 40, further comprising applying a signal to a word line and a bit

2         line of the second block to read the memory cell substantially simultaneously with

3         erasing the first block.

1    43. The method of claim 40, wherein said receiving a signal to erase a first block within a

2         memory array comprises:

3                 receiving an instruction to erase the first block; and

4                 receiving an instruction to read the memory cell prior to erasure of the first

5         block.

1    44. The method of claim 40, wherein said lowering an output of a negative charge pump to

2         a negative voltage comprises lowering the output of the negative charge pump to a

3         high magnitude, negative voltage.

1    45. The method of claim 40, wherein said applying the output of the negative charge pump

2         to a source line of the first block comprises coupling the output of the negative charge

3         pump to the source line.

1    46. The method of claim 40, wherein said pulling up the output comprises turning off

2         transistors to substantially prevent current burn within a negative level shifter coupled

3         to the second block of memory.

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47. The method of claim 40, wherein said pulling up the output comprises applying a low resistance current to the memory cell.

1    48. An apparatus, comprising:

2                 a negative charge pump; and

3                 a block controller coupled to the negative charge pump, comprising:

4                         a negative level shifter to switch an output between a read-mode

5                         voltage and an erase-mode voltage dependent upon a selection

6                         signal input; and

7                 a positive voltage switch coupled to the negative level shifter.

1    49. The apparatus of claim 48, wherein the negative level shifter comprises an output stage

2                 circuit to couple to said negative charge pump to output the erase-mode voltage.

1    50. The apparatus of claim 48, wherein the negative level shifter comprises a first circuit

2                 to pull up an output of said negative charge pump to output a read-mode voltage.

1    51. The apparatus of claim 50, further comprising a second negative level shifter to couple

2                 to said negative charge pump to output an erase-mode voltage substantially

3                 simultaneously with an output of the read-mode voltage by the negative level shifter.